PATENT

Atty Docket No.: 10004808-1
Appl. Ser. No.: 09/891,324

REMARKS

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. By virtue of the amendments above, Claim 1 has been amended and Claims 14-20 have been added. As such, Claims 1-20 are currently pending, of which, Claims 1, 14 and 20 are independent.

No new matter has been introduced by way of the claim amendment or additions; entry thereof is therefore respectfully requested.

Prosecution Re-opened Following Appeal Brief Filing

The Official Action dated May 24, 2006 re-opens prosecution on the merits of the present application following the filing of an Appeal Brief on November 14, 2005. In re-opening prosecution, the Official Action relies upon a newly introduced document, U.S. Patent No. 6,617,206 to Sandhu et al., having a filing date of June 7, 2000 and a patent date of September 9, 2003.

Claim Rejection Under 35 U.S.C. §102

Claims 1-13 have been rejected under 35 U.S.C. §102(b) as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 6,617,206 to Sandhu et al. For at least the following reasons, it is respectfully submitted that this rejection is clearly improper and should be withdrawn.

Sandhu et al. Fails to Qualify Under 35 U.S.C. §102(b)

Section 102(b) of United States Code 35 states that:

> A person shall be entitled to a patent unless – ...

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Sandhu et al. fails to qualify as a reference under 35 U.S.C. §102(b) because the present application was filed prior to the Sandhu et al. patent date. More particularly, Sandhu et al. has a patent date of September 9, 2003 and the present application has a filing date of June 27, 2001.

Accordingly, the rejection of Claims 1-13 as allegedly being unpatentable under 35 U.S.C. §102(b) based upon Sandhu et al. is clearly improper and should be withdrawn.

Sandhu et al. Fails to Anticipate the Claimed Invention

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

Sandhu et al. Fails To At Least Disclose That the Second Electrode is in Direct Contact With the Substantially Thin Insulator Layer

Claim 1 of the present invention pertains to a method of forming a by-pass capacitor on a multi-level metallization device (100), as shown in the flow diagram (200) depicted in Figure 2. The steps outlined in the flow diagram (200) are further illustrated with respect to Figures 3A-3E, which depict side views during various stages of the claimed multi-level metallization device (100) formation process.

In the method of Claim 1, a first electrode (320-324) is formed in a first dielectric layer (305) of the multi-level metallization device (100). This element of Claim 1 is depicted at step 210 of Figure 2, in Figure 3A, and a description of this element is set forth in line 14 of page 7 to line 2 of page 8 in the *Specification*. Claim 1 also recites that a substantially thin insulator layer (330) is deposited over the first dielectric layer (305) of the multi-level metallization device (100). This feature of Claim 1 is depicted at step 215 of Figure 2, in Figure 3B, and a description of this element is set forth in lines 3-12 of page 8 of the *Specification*.

Claim 1 further recites that a second electrode (360) is formed in a second dielectric layer (335), wherein the second dielectric layer (335) is formed over the substantially thin insulator layer (330). This feature of Claim 1 is depicted at step 235 of Figure 2, in Figure 3E, and a description of this element is set forth in the paragraph starting on line 21 of page 8 and ending on line 2 of page 9 of the *Specification*.

In addition, Claim 1 has been amended to recite that the second electrode (360) is formed such that the second electrode (360) is in direct contact with the substantially thin insulator layer (330). This feature of Claim 1 is depicted in Figure 3E.

Sandhu et al. discloses a method of forming a capacitor structure. In forming the capacitor structure, Sandhu et al. discloses that a "high-K dielectric is deposited in a series of thin layers and oxidized in a series of oxidation steps". (Abstract). Sandhu et al. asserts that the use of the series of thin dielectric layers as opposed to a single larger dielectric layer is beneficial because this configuration enables the layer nearest the capacitor electrode to be formed under less aggressive oxidizing parameters. (column 2, lines 54-61).

The Official Action asserts that Figure 3B of Sandhu et al. discloses all of the features of Claim 1. More particularly, the Official Action asserts that either of the dielectric layers 18 and 19 reads on the claimed first dielectric layer and that the conductive layer 20 reads on the claimed first electrode. The Official Action also asserts that the first layer 22 of capacitor dielectric 24 reads on the claimed substantially thin dielectric layer. The Official Action further asserts that the second layer 23 of capacitor dielectric 24 reads on the claimed second dielectric layer and that the conductive layer 25 reads on the claimed second electrode.

Turning now to Figure 3B of Sandhu et al., the second layer 23 of the capacitor dielectric 24 is depicted as being formed on top of the first layer 22 of the capacitor dielectric 24. Sandhu et al. also discloses that the second layer 23 is formed on top of the first layer 22 through "chemical-vapor-deposition (CVD), physical-vapor-deposition (PVD), jet-vapor deposition (JVD), liquid deposition (e.g., spin-on, liquid injection, and the like..." (column 5, lines 9-15 and see column 6, lines 46-50, where Sandhu et al. states that the second layer 23 is formed in a manner similar to the first layer 22).

As such, Sandhu et al. discloses that both the first layer 22 and the second layer 23 are formed of relatively thin layers of capacitor dielectric material for reasons as stated above. In this regard, for instance, the Official Action's assertion that the conductive layer 25 is formed in the second layer 22 is clearly improper. More particularly, because the second layer 23 is

formed of the thin layer of capacitor dielectric material, the conductive layer 25 cannot reasonably be construed as being formed in the second layer 23. Instead, as shown in Figure 3B, the conductive layer 25 is formed **on top** of the second layer 23. In addition, because Sandhu et al. discloses that the second layer 23 is formed through various deposition processes (column 5, lines 9-15), Sandhu et al. also fails to disclose that the second layer 23 would be etched to receive the conductive layer 25. Instead, Sandhu et al. discloses that the dielectric layers 18 and 19 are etched (column 3, lines 50-53) to form holes, into which the first layer 22, the second layer 23, and the conductive layers 20 and 25 are deposited. As such, the second layer 23 conforms to the shapes of the holes and the conductive layer 25 rests on top of the second layer 23 and not inside of the second layer 23.

Moreover, therefore, because the conductive layer 25 is formed on top of the second layer 23, the conductive layer 25 cannot reasonably be construed as being in direct contact with the first layer 22. In other words, Sandhu et al. clearly fails to disclose that the second electrode is in direct contact with the substantially thin insulator layer as claimed in Claim 1 of the present invention.

For at least the foregoing reasons, it is respectfully submitted that Sandhu et al. fails to disclose each and every element claimed in independent Claim 1 of the present invention and therefore cannot anticipate this claim. The Examiner is therefore respectfully requested to withdraw this rejection and to allow Claim 1 and the claims that depend therefrom.

Sandhu et al. Fails To At Least Disclose That At Least One Via Is Etched Into the Second Dielectric Layer As Claimed In Claim 7

The Official Action asserts that the disclosure contained in column 3, lines 50-55 of Sandhu et al. teaches that a via is etched to receive the second electrode. It is respectfully

submitted that this assertion is incorrect because column 3, lines 50-55 of Sandhu et al. discusses that "[d]ielectric layers 18 and 19 are deposited and etched to provide holes of deposition of conductive layer 20." Conductive layer 20 has been construed in the Official Action as reading on the claimed first electrode and conductive layer 25 has been construed as reading on the claimed second electrode.

As such, Sandhu et al. discloses that the first dielectric layer (dielectric layers 18 or 19) is etched to receive the first electrode 22 (conductive layer 20). Therefore, Sandhu et al. fails to disclose that at least one via is etched in the second dielectric layer (second layer 22) and is adapted to receive the second electrode (conductive layer 25).

Newly Added Claims

Claims 14-20 have been added to further define the scope of the invention. Claims 14-20 are allowable over the cited references of record for at least the reasons set forth above with respect to Claim 1. Claims 14 and 20 are further allowable over Sandhu et al. because Sandhu et al. fails to disclose that at least one via is etched in the second dielectric layer, where the at least one via extends through the second dielectric layer to the substantially thin insulator layer. In addition, Sandhu et al. fails to disclose that metal is deposited into the at least on via to form a second electrode. Claims 15 and 20 are further allowable over Sandhu et al. because Sandhu et al. fails to disclose that the second electrode is in direct contact with the substantially thin insulator layer.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

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Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

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Dated: August 24, 2006

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